Address	Gating Waveforms	Package References		
		AND Gate	Line & Inverter	Output Delay
0.0.	$N10_0$, N20	38D4	39C	38C2
0.1.	$N10_0$, N21	38D3	39D	"
0.2.	$N10_0$, N22	38D2	37C	38C1
0.3.	$N10_0$, N23	38D1	37D	"
0.4.	$N10_1$, N24	37H4	37E	37G2
0.5.	$N10_1$, N25	37H3	37F	"
0.6.	$N10_1$, N26	37H2	37J	37G1
0.7.	$N10_1$, N27	37H1	37K	"
1.0.	$N11_0$, N20	38H4	38E	38G2
1.1.	$N11_0$, N21	38H3	38F	"
1.2.	$N11_0$, N22	38H2	38J	38G1
1.3.	$N11_0$, N23	38H1	38K	"
1.4.	$N11_1$, N24	39H4	39E	39G2
1.5.	$N11_1$, N25	39H3	39F	"
1.6.	$N11_1$, N26	39H2	39J	39G1
1.7.	$N11_1$, N27	39H1	39K	"
2.0.	$N12_0$, N20	39Q4	39L	39P2
2.1.	$N12_0$, N21	39Q3	39M	"
2.2.	$N12_0$, N22	39Q2	39R	39P1
2.3.	$N12_0$, N23	39Q1	39S	"
2.4.	$N12_1$, N24	39W4	39T	39V2
2.5.	$N12_1$, N25	39W3	39U	"
2.6.	$N12_1$, N26	39W2	39X	39V1
2.7.	$N12_1$, N27	39W1	39Y	"
3.0.	$N13_0$, N20	38Q4	38L	38P2
3.1.	$N13_0$, N21	38Q3	38M	"
3.2.	$N13_0$, N22	38Q2	38R	38P1
3.3.	$N13_0$, N23	38Q1	38S	"
3.4.	$N13_1$, N24	38W4	38T	38V2
3.5.	$N13_1$, N25	38W3	38U	"
3.6.	$N13_1$, N26	38W2	38X	38V1
3.7.	$N13_1$, N27	38W1	38Y	"

ORDINARY REGISTERS

ADDRESS CODING FOR COMPUTING STORE

N0x Accumulators and Special Register Blocks

N1y Ordinary Register Blocks

N2z Position Within Block

Examples:

Decoding	Octal Number	Decimal Number	Address	Type
N13 N25	135	93	3.5	Ordinary Register
N00 N21	01	1	1	Accumulator
N01 N27	17	15	15	Special Reg. Handkeys
N02 N21	21	17	17	Unchecked Input or Output
N04 N22	42	34	34	Constant (= 2^{-10})

Address	Gating Waveforms	Package References		
		AND Gate	Line & Inverter	Output Delay
4.0.	N14, N20	37Q4	37L	37P2
4.1.	N14, N21	37Q3	37M	"
4.2.	N14, N22	37Q2	37R	37P1
4.3.	N14, N23	37Q1	37S	"
4.4.	N14, N24	37W4	37T	37V2
4.5.	N14, N25	37W3	37U	"
4.6.	N14, N26	37W2	37X	37V1
4.7.	N14, N27	37W1	37Y	"
5.0.	N15, N20	36Q4	36L	36P2
5.1.	N15, N21	36Q3	36M	"
5.2.	N15, N22	36Q2	36R	36P1
5.3.	N15, N23	36Q1	36S	"
5.4.	N15, N24	36W4	36T	36V2
5.5.	N15, N25	36W3	36U	"
5.6.	N15, N26	36W2	36X	36V1
5.7.	N15, N27	36W1	36Y	"

ADDRESS DECODING

Repeater	Input	Output
35Y3	$N10_0$	$N10_1$
35Y4	$N11_0$	$N11_1$
35Y5	$N12_0$	$N12_1$
35Y1	$N13_0$	$N13_1$
34X6	$S10_0$	$S10_1$
34E3	$\sim S10_0$	$\sim S10_1$

INPUT BUS

Repeater	Output	Destinations
-	$Y35_0$	Parity circuit and all repeaters
34E5	$Y35_1$	Block 1 and first half of block 0
34X4	$Y35_2$	Block 2 and second half of block 3
34X5	$Y35_3$	Block 5 and second half of block 4
34P5	$Y35_4$	First half of blocks 3 and 4. Second half of block 0
34P4	$Y35_5$	All accumulators (modifier by-pass)
33F3 (AND gate)	$Y35_6$	All accumulators (normal input)
20D5	$Y35_7$	Output (punch) circuit ('Mix' output to parity circuit)

REPEATERS

FIG. 10. 7 TABULATED DETAILS